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EXAMINER
GOSSAGE, GLENN A

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/586,145	KATSETOS ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --METHODS FOR INTERFACING COMPONENTS AND FOR WRITING AND READING A SERIAL DATA STREAM TO AND FROM A COMPONENT ASSOCIATED WITH A PARALLEL DATA STREAM-- is suggested (see claims 1, 10 and 16, line 1, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because the abstract does not enable one to quickly determine from a cursory inspection the nature and gist of the entire technical disclosure as required by 37 CFR 1.72(b). It appears the abstract should be selectively rewritten to describe additionally claimed and disclosed features, while remaining within the 150 word or 15 line limit to the abstract.

[For example, in lines 1-2, change "is provided that includes the steps of receiving from a first component" to simply --includes receiving--; in lines 2-4, delete "comprising ... component"; and in line 4, change "the" to --a--. In lines 5-8, change ", the memory being ... operation. Modified data" to --, such as a cache. Data may be--. In line 10, change "the second component" to --a second one of the components--, and delete "data is." In line 11, change "the first" to --a first--. In line 12, after "operation." insert one or two sentences such as --The components may be an integrated device electronics (IDE) hard disk drive and a system or controller originally designed

to communicate with a modified frequency modulation (MFM) hard disk drive . Handshaking signals such as index and seek-complete signals allow the interface module to emulate operation of an MFM hard disk drive. Methods for writing and reading a serial data stream to and from a component associated with a parallel data stream are also described.-- See page 1, lines 2-4; page 14, lines 19-25; and page 25, lines 4-5, as well as claims 10-11 and 16-17.]

Appropriate correction is required. See MPEP § 608.01(b).

3. The drawings are objected to because in Figure 1, it appears the signal "Directio" should be --Direction-- for clarity and consistency (see page 6, line 14, e.g.). Also, descriptive labels should be inserted within "boxes" 30 and 20 for clarity. [For example, a label such as --Interface Module-- or --I/F Module-- should be placed within "box" 30 for clarity and consistency (see page 5, line 13, e.g.). Similarly, a label such as --System--, --System/Controller-- or --System (Controller)-- should be placed within "box" 20 for clarity and consistency (see page 5, lines 12 and 16; page 7, line 23; and page 25, lines 4 and 6, e.g.).

In Figure 2, descriptive labels should be inserted within "boxes" 30 and 40 for clarity, analogous to Figure 1. [For example, a label such as --Interface Module-- or --I/F Module-- should be placed within "box" 30, and a label such as --Drive-- placed within "box" 40, for clarity and consistency (again see page 5, line 13, e.g.).] Also, it appears "IDE0" should be changed to --IDED0-- for clarity and consistency (see page 7, lines 8-9, e.g.). Additionally, the

labels for the signals "RESET," "RD" and "WR" do not appear to be consistent with those used in the specification. [Should the labels "RESET," "RD" and "WR" be changed to --WRESET--, --DIOR-- and --DIOW--, respectively? See page 7, lines 9 and 19, and page 7, lines 8, 12 and 14, and also note the objection to the specification below with respect to page 7, line 8.]

In Figure 3, descriptive labels should be inserted within "boxes" 20, 22, 26A, 26B, 28, 32 and 40 for clarity. [For example, a label such as --Control System-- or --System (MFM Controller)-- should be placed within "box" 20 for clarity and consistency (see page 7, line 23, e.g.). A label such as --ROM (EPROM)-- should be placed within "box" 26B for clarity and consistency (see page 8, lines 9 and 19, as well as Figure 4, e.g.). Similarly, labels such as --Proc.--, RAM--, Cache--, --Mgmt. Module-- and --IDE Drive-- should be placed within "boxes" 22, 26A, 28 and 32, respectively, for clarity and consistency (see page 7, line 30; page 8, lines 8-9; page 8, line 9; page 8, line 1; and page 7, line 26, for example).] A label such as --I/F Module-- may also be placed near (to the right of, e.g.) reference numeral 30 for clarity.

In Figure 4, it is not entirely clear whether "Page" (all occurrences) should be changed to --Block-- for clarity and consistency (see page 8, lines 24-25 and 30, e.g.).

In Figure 5, descriptive labels should be inserted within "boxes" 20, 22, 28, 32 and 64 for clarity, similar to Figure 3. [For example, a label such as --System-- or --Control System-- should be placed within "box" 20 for clarity (see page 9, line 12, e.g.). Similarly, labels such as --Drive--, --Proc.--, Cache-- and --Mgmt. Module-- should be placed within "boxes" 40, 22, 28 and 32, respectively, for clarity and consistency (see page 9, line 13; page 9, line 17; page 9, line

18; and page 9, line 19, for example). The "box" 64 within the management module 32 should also be descriptively labeled for clarity (--Cache Arbit.--? Note "box" 64 in Figure 9. A label such as --I/F Module-- may also be placed near (to the right of, e.g.) reference numeral 30 for clarity.]

In Figure 6A, within "box" or step 1602, it appears --Drive-- should be inserted after "IDE" for clarity and consistency (see page 10, line 4, e.g.).

In Figure 6C, within "box" or step 642, "Ram" should be --RAM Cache-- for clarity and consistency (see page 10, lines 26-27, e.g.).

In Figure 8A, within "box" or step 800, it appears --Cache-- should be inserted before "Interrupt" for clarity and consistency (see page 12, line 4, e.g.). In "box" or steps 808, 816 and 820, it appears --Drive-- should be inserted after "IDE" for clarity and consistency (see page 12, line 4, e.g.). See also "box" or step 832 in Figure 8B.

In Figure 9, within "box" or block 62, it appears --RAM-- should be inserted after "Cylinder" for clarity and consistency (see page 17, lines 20-24, as well as the label within "box" or block 58, e.g.). Also, within "box" or block 94, it appears "stat" should be --Status-- for clarity and consistency (see page 23, line 6, e.g.).

In Figure 10, within "box" or step 118, it appears --Send-- should be inserted before "Drive" for clarity (the drive ready signal is sent, not released) and consistency (see page 23, line 30, e.g.). In "boxes" or steps 120 and 136, it appears --Cache-- should be inserted before "Interrupt" for clarity and consistency (see page 24, lines 1-2, e.g.).

In Figure 11A, within decision step or "box" 212, it appears --Requested-- should be inserted after "Address 0" for clarity and consistency (see page 24, lines 14-15, e.g.).

In Figure 13, descriptive labels should be inserted within "boxes" 20, 30 and 40 for clarity, analogous to Figure 1. [For example, a label such as --System-- or --System (Controller)-- should be placed within "box" 20 for clarity and consistency (see page 25, lines 4 and 6, e.g.). Similarly, a label such as --Interface Module-- or --I/F Module-- should be placed within "box" 30 (note page 25, line 6, e.g.), and a label such as --Drive-- placed within "box" 40, for clarity and consistency (see page 25, line 8, e.g.).]

In Figure 14, many of the labels are too small and cannot be read. Also, many of these labels do not appear to be relevant to the present claimed. Accordingly, the labels shown in Figure 14 which are not relevant to the present invention should be deleted for clarity.

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) (submission of corrected formal drawings, e.g.) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

4. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any

errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, lines 3 and 4, and throughout the specification, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well known." Accordingly, "IDE" and "MFM" should be changed to --integrated device electronics (IDE)-- and --modified frequency modulation (MFM)--, respectively, for clarity (note page 2, lines 2 and 4-5, e.g.). See also page 1, line 7; page 12, line 25; and page 14, lines 26 and 29, by way of example only.

On page 3, line 6, "and" appears to read clearly here as --the request--. In line 22, it appears "A" should be --The--.

On page 4, line 3, it appears --a-- should be inserted before "computer." In lines 19 and 23, respectively, it appears "Figure 6 (8) is an illustration of" should be changed to --Figures 6A-6C (8A-8B) illustrate-- or other similar language for clarity.

Similarly, on page 5, lines 1 and 3, respectively, it appears "Figure 11 (12) is" should be changed to --Figures 11A-11C (12A-12C) illustrate-- or other similar language for clarity.

On page 5, line 13, it appears "referred to collectively" should be changed to --shown collectively in Figure 2-- for clarity.

On page 6, line 14, it appears --MFM-- should be inserted before "write" for clarity and consistency (see page 5, line 24, e.g.). In line 22, it appears "spin" reads more clearly and consistently here as --move-- (see lines 23 and 24).

On page 7, line 8, the labels "DIOW" and "DIOR" are not entirely clear here, when read in conjunction with Figure 2. [Should --(WR)-- and --(RD)-- be inserted after "DIOW" and "DIOR," respectively?] In this regard, also note the drawing objection above with respect to Figure 2.

On page 8, line 7, "MHZ" should be --megahertz (MHZ)-- for clarity. In lines 18 and 19, the use of different names or labels for the same reference numeral (ROM 26B and EPROM 26B) is confusing. It appears "EPROM 26B" in line 19 should be changed to --The EPROM or ROM 26B-- for clarity. [In this regard, note the drawing objection and suggestion above with respect to the labeling of "box" 26B in Figure 3.] In lines 23 and 25, and throughout the specification, the repeated use of different names or labels for the same reference numeral (cache 28 and cylinder RAM 28) is confusing. See also page 9, lines 3, 6, 10, 15 and 26, by way of example only. It appears an explanatory sentence or parenthetical phrase should be added for clarity. [For example, on page 8, line 25, after "D).", insert a sentence or phrase such as --Reference numeral 28 may be referred to hereafter as cache 28 or cylinder RAM 28.--].

On page 9, line 5, it appears "and" should be deleted for clarity. In lines 14 and 21, it appears --in Fig. 9-- should be inserted after "62" for clarity. In line 20, it appears --below-- should be inserted after "discussion" for clarity. Also, it appears the "box" 64 shown within the

management module 32 in Figure 5 should be described here, at least briefly, for clarity and completeness.

On page 10, line 3, "Figure 6" should be changed to --Figures 6A-6C-- for clarity. In line 4, it appears --IDE-- should be inserted before "drive" for clarity and consistency (see step 602 in Figure 6A, e.g.). In line 18, "LED" should be written out as --light emitting diode (LED)-- for clarity (see page 23, line 7, and again note that the first occurrence of all acronyms or abbreviations should be written out for clarity).

On page 11, in lines 7-8, the brief discussion or mention of steps 702-710, which make up a large part of Figure 7, is not sufficiently clear and descriptive.

On page 12, line 3, "Figure 8" should be changed to --Figures 8A-8B-- for clarity. In line 4, it appears --IDE-- should be inserted before "drive" for clarity and consistency (see step 800 in Figure 8A, e.g.). In line 26, it appears --component-- should be inserted after "single" for clarity. In line 29, it appears "by the" should be simply --by--.

On page 13, line 24, it appears --below-- should be inserted after "1" for clarity. In line 26, it is not entirely clear whether --A0,-- should be inserted before "A1" (see Table 1 on page 14, e.g.). In line 27, the wording "is selected, IO" is confusing. [Should ", IO" in line 27 be deleted, and --IO-- inserted after "pin" in line 26?]

On page 15, line 7, it appears --(Fig. 3)-- should be inserted after "28" for clarity.

On page 18, line 5, it appears "as a" should be --as an--. In line 19, it appears "XNOR" should be --exclusive NOR (XNOR)-- for clarity.

On page 19, lines 4-5, the wording "involving functions such as synchronize data, write channel, read channel, and address counter" is idiomatically awkward and confusing. In line 24, "74191" is not adequately clear in this context. In line 27, "dig-" should be --digital-- for clarity and consistency (see page 14, line 15, e.g.).

On page 20, paragraph 2, at line 4 of the paragraph, it appears "100ns" should be --100 nanoseconds (ns)-- for clarity.

On page 21, lines 21 and 22, it appears "hi" should be --high-- for consistency (see Fig. 9). See also page 22, line 26 (two occurrences).

On page 22, line 29, it is not entirely clear to what a "sheet" (of blocks) refers here.

On page 23, line 26, "after" appears to read more clearly here as --where--.

On page 24, lines 12 and 26, respectively, "Figure 11 (12)" should be changed to --Figures 11A-11C (12A-12C)-- for clarity and consistency. In lines 20 and 22, it appears --(Fig. 11B)-- and --(Fig. 11C)-- should be inserted after "250" and "252," respectively, for clarity. In line 26, it appears "this figure" should be --these Figures-- for clarity.

Additionally, in lines 18-19, the brief discussion or mention of steps 228-246, which make up a large part of Figure 11B, is not sufficiently clear and descriptive. Similarly, in lines 28-29, the brief mention of steps 312-324 and 326-342, which make up a large part of Figure 12A-12B, is not sufficiently clear and descriptive.

On page 25, line 1, it appears --(Fig. 12B)-- and --(Fig. 12C)-- should be inserted after "346" and "348," respectively, for clarity. In line 19, it is not clear what is meant by "at least about."

It appears "at least" should simply be deleted for clarity. In lines 28 and 29, respectively, it appears "(J1)" and "(J2)" should be deleted since these labels do not appear to be shown, at least visibly, in Figure 14.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 1, lines 2 and 4, respectively, --first-- and --second-- should be inserted before "communication" for clarity. In line 6, "and" appears to read more clearly here as --the request--. In line 14, it appears "the data" should be simply --data-- for clarity and consistency (see page 3, lines 13-14, e.g.).

In claim 2, line 2, it appears --stored-- should be inserted before "in" for clarity and consistency (see claim 3, line 2, e.g.). Also, it appears "step" in line 3 should be --steps-- for clarity and consistency (note claim 20, line 3, e.g.). Also, "comprises" in line 4 should be changed to --respectively comprise--. In line 5, it appears --for an access operation-- should be inserted after "request" for consistency (see claim 1, line 5).

In claim 3, line 3, "stored data currently" appears to read more clearly here as --data currently stored--.

In claim 6, line 5, the wording "which within the oldest page" is not clear. [Should "which" be moved after "page?"]

In claim 8, line 2, it appears --said method-- should be inserted before "further" for clarity.

Similarly, in claim 9, line 2, it appears --said method further comprising-- should be inserted after "stream," for clarity.

In claim 10, line 3, it appears "a" should be --the-- to avoid possible antecedent problems (note lines 1 and 3, as well as the reference to "the serial data stream" in claim 12, line 3, e.g.). Similarly, in line 5, it appears --converted from the serial data stream-- should be inserted after "stream" for clarity (to avoid possible antecedent problems, e.g. Note the plural "parallel data streams" set forth in claim 10, lines 1-2, e.g.). In line 6, it appears "a" should be --the-- (note line 1).

In claim 11, line 2, it appears --(IDE)-- should be inserted after "electronics" and --drive-- inserted after "disk" for clarity. Also, it appears "a" should be --the--. In line 4, it appears --(MFM)-- should be inserted after "modulation" for clarity.

In claim 12, line 6, it appears --loaded in the memory-- should be inserted after "stream" to avoid possible antecedent problems.

In claim 14, line 2, it appears "a" should be --from the memory to the-- for clarity and consistency (note claim 10, line 6, e.g.).

In claim 16, line 4, it appears "for the" should be simply --for--. In line 6, it appears --received-- should be inserted before "parallel" and "a" changed to --the-- to avoid possible antecedent problems).

In claim 17, line 2, it appears --(IDE)-- should be inserted after "electronics" and --drive-- inserted after "disk" for clarity. Also, it appears --received-- should be inserted before "parallel" in claim 17, lines 2 and 3, as well as claim 18, lines 1 and 3, for clarity (to avoid possible antecedent problems, e.g., since there are plural parallel data streams set forth in claim 16, line 2). In line 4, it appears --(MFM)-- should be inserted after "modulation" for clarity.

Also in claim 18, line 2, "a" should be --the--.

In claim 19, line 3, it appears "the data" reads more clearly here as --requested data-- (note claim 1, lines 8-9, as well as claim 19, line 5, e.g.). In line 6, it appears --missing-- should be inserted before "data" to avoid possible antecedent problems. See also claim 20, lines 3 and 6.

In claim 20, line 2, it appears --requested-- should be inserted before "data" (both occurrences) for clarity and consistency (note claim 19, line 5). In line 4, it appears "comprises" should be --respectively comprise-- analogous to claim 2, line 4. In line 5, it appears --for data-- should be inserted after "request" for clarity and consistency (note claim 16, line 3 e.g.).

In claim 21, lines 2-3, it appears " , wherein ... loaded" should be deleted.

In claim 25, line 2, it appears "further" should be deleted, and --for data-- inserted after "request" for clarity and consistency.

In claim 30, line 1, it appears --stream-- should be inserted after "data" for consistency.

In claim 33, line 2, it appears "to the component" should be moved after "writing" in line 1 for clarity. In line 2, "prior" should be -- , prior-- for clarity.

Appropriate correction is required.

5. Claims 14, 19, 20, 25-28 and 31-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, it is not adequately clear what is meant by "convenient" (to the processor) here (support for language in the specification?). Compare the clearer language of claim 15, lines 3-4, e.g.

In claim 19, and therefore claims 20, 25-28 and 31-33 dependent therefrom, it is not clear how the method is to be "interrupted" or "resumed" (the "interrupting" and "resuming" would appear to be a part of the method itself).

In claim 28, it is not entirely clear how the step of "resuming" the method is to be implemented here analogous to claim 19.

Also In claims 32 and 33, it is not clear ho w a "portion" of memory "is older than" another portion. [Should "that is older than" in claim 32, line 2 be changed to --storing data that is older than data stored in--, and "the oldest portion (of the memory)" in claim 33, lines 2 and 2-3 be changed to --the portion of the memory storing the oldest data--?]

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-37 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-9 of U.S. Patent No. 6,546,348. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned patent claims a system for interfacing a first component and a second component, the first component being associated with a first electrical interface and

communication type, and the second component being associated with a second electrical interface and communication type, the system including a management module being configured to receive from the first component a request for an access operation comprising one of at least a write operation and a read operation, and involving a requested data address associated with the second component, and to determine whether data corresponding to the requested data address is missing from memory, the memory being independent of the second component, as in the claimed invention (see claim 1, lines 1-6 and 11-17 of the patent, e.g.).

In the system of the commonly assigned patent, when the data is missing from the memory, the management module is further configured to interrupt the access operation, load the data from the second component to the memory, and perform the access operation (see claim 1, lines 18-22 of the patent, e.g.). Modified data is converted from the first communication type to the second communication type and written over the data in the memory and in the component during a write operation, and wherein the data is converted from the second communication type to the first communication type and read by the first component during a read operation (see claim 1, lines 22-29 of the patent and present claim 1, e.g.).

The commonly assigned patent also claims interrupting and resuming the access operation (see claim 1, line 18 of the patent, e.g.), and that the memory comprises cache memory such as cylinder random access memory (see claims 2 and 3 of the patent, e.g.) including a plurality of blocks, each comprising a plurality of pages (see claim 7 of the patent).

The commonly assigned patent also claims that the first component comprises a

controller having an IEEE 412 interface and the second component comprises a hard disk drive having an AT attachment (ATA) or IDE interface, and that the controller is associated with a modified frequency modulation (MFM) bit encoding specification and wherein the hard drive comprises an IDE hard drive (see claims 8 and 9 of the patent).

Thus, a method for interfacing the first component and the second component in such a system as claimed, the first component being associated with a first electrical interface and communication type and the second component being associated with a second electrical interface and communication type, would have been obvious to a person of ordinary skill in the art at the time the claimed invention was made having the claims of U.S. Patent No. 6,546,348 before him or her, anticipation being the epitome of obviousness.

With respect to claims 10-34, while the patent does not expressly state that the data that is converted is converted between a serial data stream and a parallel data stream, the patent claims interfacing a first component associated with a first electrical interface and communication type and a second component associated with a second electrical interface and communication type, and that the first component comprises a controller having an IEEE 412 interface and the second component comprises a hard disk drive having an AT attachment (ATA) or IDE interface, and that the controller is associated with a modified frequency modulation (MFM) bit encoding specification and the hard drive comprises an IDE hard drive (gain see claims 8 and 9 of the patent). As one of ordinary skill in the art would readily appreciate, a controller having an IEEE

412 interface associated with a modified frequency modulation (MFM) bit encoding specification would transfer a serial data stream, while the second component comprising a hard disk drive having an AT attachment (ATA) or IDE interface is associated with parallel data streams, and thus a method for writing and reading a serial data stream to and from a component associated with the parallel data streams, including receiving, converting, loading and outputting the data streams as claimed would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made. That is, one of ordinary skill in the art at the time the claimed invention was made having the claims of the commonly assigned patent before him or her would have found the methods of writing and reading a serial data stream to and from a component associated with parallel data streams readily obvious. Also, one of ordinary skill in the art would readily recognize that computer related inventions may be implemented in hardware and/or software, and the use of a computer readable medium to store software or instructions (see present claims 35-37, e.g.) to implement the methods would have been further readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-12, 14-18, 21-24, 29-30 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 6 to page 2, line 8 of the present specification, e.g.) in view of Kobayashi and Noll, taken together.

With respect to claims 10 and 16, applicants' admitted prior art discloses that various methods for writing and reading to and from storage devices such as hard drives in a computer system were well known in the art at the time the claimed invention was made. The hard drives typically are manufactured to operate so as to be compliant with industry standards formats or protocols so as to be compatible with a large number of devices. However, the usefulness of controllers designed for older interfaces or standards such as the IEEE 412 or ST506 standard which utilizes a serial data stream has diminished as storage devices or hard drives complying with the newer ATA or IDE standard which use a parallel interface have gained wider acceptance (see page 1, line 6 to page 2, line 8, e.g.).

Kobayashi similarly discloses various methods for reading and writing data to and from devices such as hard drive controllers and storage devices, and teaches converting between a serial stream or standard and a parallel standard or protocol such as the ATA standard. Kobayashi discusses converting from a universal serial bus protocol to an ATA or IDE standard or protocol, but also discusses that the teachings are applicable with equal effect to the case where different serial and parallel standards are converted to each other, and is widely applicable to the case in which the peripheral equipment of the computer are controlled (see column 14, lines 11-20). Kobayashi also teaches that since many existing are based on the ATA standard, by

converting between the serial protocol or standard of the controller or computer and the parallel ATA standard of the storage device, compatibility with existing devices may be maintained (see column 2, line 55 to column 3, line 19, as well as column 6, lines 14-17, and column 10, lines 15-20, e.g.).

Noll similarly discloses methods for reading and writing between devices utilizing different industry standards or protocols. Noll teaches that IDE drives which are compliant with the ATA industry standard have achieved similar densities at similar access times than other industry standard drives, and also teaches that such IDE or ATA drives are typically cheaper and smaller than drives such as SCSI drives. Noll further teaches that it would be desirable to be able to connect an IDE hard drive with an older controller or bus standard to take advantage of the smaller size and lower price with comparable storage capacities and access times (see column 2, lines 45-53 and column 8, lines 1-6, e.g.). Noll also teaches utilizing a buffer or memory when interfacing the two different standards or when transferring data to and from the IDE drive (see column 8, lines 1-6, e.g.).

One of ordinary skill in the art at the time the claimed invention was made having the teachings of Kobayashi and Noll before him or her would have found it readily obvious to provide an interface and convert between a serial stream or standard and a parallel standard or protocol such as the ATA standard, as taught by Kobayashi, in a system having a controller utilizing serial data streams such as in applicants' admitted prior art, in order to provide compatibility with a large number of industry standard devices, particularly in light of the

discussion in Kobayashi that the teachings are applicable with equal effect to the case where different serial and parallel standards are converted to each other, and is widely applicable to the case in which the peripheral equipment of the computer are controlled (see column 14, lines 11-20). The well known use of a memory or buffer in an interface so as to provide for different data rates between different devices or standards is taught by Noll (again see column 8, lines 1-6, e.g.), and the use of such a buffer or memory when converting data between a serial data stream and a parallel data stream such as in Kobayashi so as to provide for different data rates between the different devices or standards would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

With respect to claims 11 and 17, as well as claim 29, it would have been obvious to utilize an integrated device electronics (IDE) hard disk drive because of its wide industry acceptance and because Noll teaches that it would be desirable to be able to utilize an IDE hard drive to take advantage of the smaller size and lower price with comparable storage capacities and access times. Similarly, the use of a converter with a serial data stream encoded according to the modified frequency modulation (MFM) specification would have been obvious since this standard or protocol was widely used in the industry and would provide for compatibility with a large number of devices.

With respect to claims 12 and 18, the use of a serial-to-parallel register to quickly and easily perform serial to parallel conversion with a minimum number of components as well as the use of a synchronization signal in conjunction with a serial data stream to synchronize data input and

output to a clock or other signal were well known in the art at the time the claimed invention was made, and the use such circuitry to perform the serial to parallel conversion in the methods of applicants' admitted prior art in view of Kobayashi and Noll, taken together, as discussed above, would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct.

With respect to claim 14, as well as claims 21 and 30, a processor or controller will read and write data during a time frame that is "convenient" for the processor. The data may be loaded from the hard drive to the buffer memory or cache without processor intervention. Note that Kobayashi teaches utilizing commands which may be processed uniquely by the converter (see column 3, lines 48-53, e.g.) so as to increase operating speed.

As per claims 15 and 24, it would have been obvious to perform coherency maintenance operations and write modified or "dirty" data from the memory to the component when the component is idle so as not to interfere with host access to the component (hard drive), thereby avoiding conflicts and the need for arbitrating access to the component (hard drive). An interrupt may be generated

With respect to claims 22 and 23, the data rates or clock frequency may obviously be adjusted and the selection of a particular speed or frequency does not render the claimed invention patentably distinct.

As per claim 29, data may be repeatedly out in the system of applicants' admitted prior art in view of Kobayashi and Noll as discussed above, with an index pulse being used to delineate the

tracks of data consistent with serial data transfer from a disk having plural tracks in a well known manner.

With respect to claims 36 and 37, one of ordinary skill in the art would recognize that computer related inventions may be implemented in hardware and/or software and the use of a computer readable medium storing instructions for implementing the above methods would have been readily obvious to one of ordinary skill in the art.

8. Claims 13, 19-20, 25-28 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 6 to page 2, line 8 of the present specification, e.g.) in view of Kobayashi and Noll, taken together, as applied to claims 10-12, 14-18, 21-24, 29-30 and 36-37 above, and further in view of Weber et al.

With respect to claim 13, applicants' admitted prior art in view of Kobayashi and Noll, taken together, discloses an interface and methods for transferring data between devices having different industry standards or protocols including serial to parallel and parallel to serial conversion and a buffer memory (see numbered paragraph 7 above), but does not teach that the buffer used in conjunction with the serial to parallel and parallel to serial conversion is a cache buffer memory.

Weber et al similarly discloses an interface between a computer or controller including an interface using serial to parallel and parallel to serial conversion, and additionally teaches utilizing a cache buffer memory in the interface so as to provide fast access to the data stored in

the cache memory in a well known manner (see cache 36 and interface 28 in Figure 1, e.g.). Weber et al also teaches using the cache buffer with well known industry standards or protocols such as ST506 or ST412 (also known as IEEE 412) and IDE (see column 4, lines 1-6, e.g.). As one of ordinary skill in the art would appreciate, the use of a cache memory provides faster access to data stored therein so as to reduce overall access times and increase operating speed, and to prevent the controller or processor from experiencing excessive idle times due to differences in transfer rates, thereby increasing overall throughput (see column 1, lines 27-51, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to utilize a cache buffer memory in conjunction with an interface between a disk drive and a controller, as taught by Weber et al, in the methods of reading and writing of applicants' admitted prior art in view of Kobayashi and Noll, taken together, as previously discussed, in order to reduce overall access times and increase operating speed, and to prevent the controller or processor from experiencing excessive idle times due to differences in transfer rates.

With respect to claims 19-20 and 31, Weber et al also teaches checking if there is a cache "miss" (determining whether data is "missing" from the cache) and loading data from the component (hard drive) to the cache when the data is "missing from the cache (see column 1, lines 41-54, e.g.). The data may be output "substantially" immediately after the data is found to be in the memory to reduce delays.

With respect to claims 25-26 and 28, it would have been obvious to utilize an integrated device electronics (IDE) hard disk drive because of its wide industry acceptance and because Noll teaches that it would be desirable to be able to utilize an IDE hard drive to take advantage of the smaller size and lower price with comparable storage capacities and access times, as discussed above with respect to claims 11 and 17. Similarly, the use of a converter with a serial data stream encoded according to the modified frequency modulation (MFM) specification would have been obvious since this standard or protocol was widely used in the industry and would provide for compatibility with a large number of devices. Since MFM encoding and an ST506 or ST412 standard or protocol is being used, it would be necessary to use handshaking signals such as a seek complete signal or line for compliance with the protocol or standard.

With respect to claim 27, a processor or other controller may be used to transfer data between the component (hard drive) and the cache or buffer in a well known manner.

With respect to claims 32 and 33, Weber et al teaches writing data over or evicting data from the cache based on age (see column 5, lines 65-68, e.g.), and the use of a cache replacement scheme such as least recently used (LRU) to maintain the newest data in the cache memory would have been readily obvious to one of ordinary skill in the art.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nissimov et al is cited as discussing disk drive interfaces utilizing parallel-to-serial conversion and as discussing providing an adapter board for converting signals between first and second formats for improved compatibility similar to the present invention (see column 1, lines 33-68).

Bonke et al is cited as disclosing a multi-drive controller including a buffer memory and a plurality of interfaces for interfacing a computer to various storage devices.

Markvoort et al is cited as disclosing a method of accessing a storage device having an interface using parallel-to-serial conversion.

Jigour et al is cited as disclosing a method of writing to a component "associated with" parallel data streams using a program buffer and a serial protocol interface (note column 3, lines 59+ and Figure 1, e.g.).

Luke et al is cited as disclosing an interface which receives a serial data stream and converts data and commands between a serial format or protocol and a parallel format or protocol to provide improved compatibility, and as also disclosing transferring data to and from an ATA device using a buffer memory (see column 1, line 63 to column 2, line 5; column 3, lines 61-67; and Figure 2, e.g.).

Watson et al and Ellis et al are cited as disclosing using a universal serial bus (USB) to parallel converter or interface and a data buffer to allow compatibility with a large number of devices.

Mizuta, published after the filing of U.S. Provisional application 60/138,080, is cited as disclosing an interface device utilizing serial-to-parallel and parallel-to-serial conversion for interfacing an ST506 interface with a hard disk drive or storage circuit similar to the present invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187